If you are using a printed copy of this procedure, and not the on-screen version, then you <u>MUST</u> make sure the dates at the bottom of the printed copy and the on-screen version match.

The on-screen version of the Collider-Accelerator Department Procedure is the Official Version.

Hard copies of all signed, official, C-A Operating Procedures are kept on file in the C-A ESHQ

Training Office, Bldg. 911A.

C-A OPERATIONS PROCEDURES MANUAL

ATTACHMENT

4.120.13.a WXY (PEER 5) CRITICAL DEVICE TESTS

C-A-OPM Procedures in which this Attachment is used.				
4.120.13				

Hand Processed Changes

HPC No.	<u>Date</u>	Page Nos.	<u>Initials</u>	
	Approved:	Signature on File		
	Coll	ider-Accelerator Departme	nt Chairman	Date

4.120.13.a WXY (PEER 5) Critical Device Tests

PASS ANNUAL ACCEPTANCE TEST PROTOCOL

Division A Software Filename and Checksum: Title:	Checksum:
Division B Software Filename and Checksum: Title:	Checksum:
<u>Initial testing complete</u> :	
Test Team Leader's Name (Print):	Life Number:
Test Team Leader's Name (Sign):	Date:/
Acceptance test procedure complete (following repairs and retesting if required):	
Test Team Leader's Name (Print):	Life Number:
Test Team Leader's Name (Sign):	Date:/
Test results reviewed by:	
Safety Section Head's Name (Print):	Life Number:
Safety Section Head's Name (Sign):	Date://
Test results accepted by Radiation Safety Committee:	
RSC Member's Name (Print):	Life Number:
RSC Member's Name (Sign):	Date:/

2

1.1 Setup and test of the Critical Devices response to a loss of PASS enable
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VERIFY	CD Key switch is set for	XY ARC
PLACE VERIFY	Peer 5 in Mode 8 Peer 5 is in Restricted Access	MODE 8
VERIFY VERIFY	MCR sees Inj CD MCR sees ATR inhibit Div A □ and Div B □	DISABLED ON
VERIFY VERIFY VERIFY	MCR sees RHIC Ring CD (B/S: □ G1, □ G2, □ G3) MCR sees RHIC Ring inhibit Div A □ and Div B □ (BS G1 and G2) MCR sees RHIC Reachback Latch inhibit Div A □ and Div B □ (BS G3)	DISABLED ON OFF
VERIFY PLACE	MCR sees ATR Reachback Latch inhibit Div A □ and Div B □ Peer 5 in Mode 16	OFF
VERIFY	Peer 5 is in Controlled Access	MODE 16
CLOSE RESET VERIFY	Peer 5 gates: UED1, WGE1, WGE2, XGI1, XGI2, YGI1 and YGI2 Peer 5 gates: WGE1, WGE2, XGI1, XGI2, YGI1 and YGI2 Peer 5 gates: WGE1, WGE2, XGI1, XGI2, YGI1 and YGI2	RESET
SWEEP VERIFY	Peer 5 Zones: W, X and Y Peer 5 Zones: W, X, and Y	SWEPT
PLACE VERIFY VERIFY VERIFY	Peer 5 in Mode 24 Peer 5 is in No Access MCR sees Inj CD MCR sees ATR inhibit Div A □ and Div B □	MODE 24 ENABLED OFF
REQUEST VERIFY	RHIC Primary Beamstop command OUT RHIC Primary Beamstop command is	OUT
VERIFY VERIFY VERIFY	MCR sees RHIC Ring CD B/S: □G1, □G2, □G3 MCR sees RHIC Ring inhibit Div A □ and Div B □ (BS G1 and G2) MCR sees RHIC Reachback Latch inhibit Div A □ and Div B □	DISABLED OFF
VERIFY	(BS G3) MCR sees ATR Reachback Latch inhibit Div A □ and Div B □	OFF OFF
TURN OFF VERIFY VERIFY VERIFY	Any key in the WXY Key Tree MCR sees Peer 5 go to MCR sees Inj CD MCR sees ATR inhibit Div A and Div B	MODE 2 DISABLED ON
VERIFY VERIFY VERIFY	MCR sees RHIC Ring CD (B/S: □ G1, □ G2, □ G3) MCR sees RHIC Ring inhibit Div A □ and Div B □ (BS G1 and G2) MCR sees RHIC Reachback Latch inhibit Div A □ and Div B □ (BS G3)	DISABLED OFF OFF
VERIFY	MCR sees ATR Reachback Latch inhibit Div A □ and Div B □	OFF
PLACE VERIFY	Peer 5 in Mode 8 Peer 5 is in Restricted Access	MODE 8

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1.2 Verify Critical Device, PSWarc20 and PSWarc8, Reachback

VERIFY	CD Key switch is set for	XY ARC
PLACE VERIFY	Peer 5 in Mode 8 Peer 5 is in Restricted Access	MODE 8
VERIFY VERIFY VERIFY VERIFY	MCR sees Inj CD on CD pg MCR sees ATR inhibit Div A □ and Div B □ MCR sees ATR Reachback Latch inhibit Div A □ and Div B □ MCR sees AGS Reachback Latch on CD pg	DISABLED ON OFF OK
REMOVE	PSWarc20 readback relay from CD Iface Box B circuit in encl 5601 in 1000P	
VERIFY VERIFY VERIFY	MCR sees Inj CD on CD pg MCR sees ATR inhibit Div A □ and Div B □ MCR sees ATR Reachback Latch inhibit Div A □ and Div B □ MCR sees AGS Reachback Latch on CD pg	DISABLED ON ON REACHBACK
REPLACE	PSWarc20 rdback relay in CD Iface Box B circuit in encl 5601 in 1000P	
RESET	Reachback	
VERIFY VERIFY VERIFY VERIFY	MCR sees Inj CD on CD pg MCR sees ATR inhibit Div A □ and Div B □ MCR sees ATR Reachback Latch inhibit Div A □ and Div B □ MCR sees AGS Reachback Latch on CD pg	DISABLED ON OFF OK
REMOVE	PSWarc8 readback relay from CD Iface Box A circuit in encl 5600 in A House	
VERIFY VERIFY VERIFY VERIFY	MCR sees Inj CD on CD pg MCR sees ATR inhibit Div A □ and Div B □ MCR sees ATR Reachback Latch inhibit Div A □ and Div B □ MCR sees AGS Reachback Latch on CD pg	DISABLED ON ON REACHBACK
REPLACE	PSWarc8 readback relay in CD Iface Box A circuit in encl 5600 in A House	
RESET	Reachback	
VERIFY VERIFY VERIFY VERIFY	MCR sees Inj CD on CD pg MCR sees ATR inhibit Div A □ and Div B □ MCR sees ATR Reachback Latch inhibit Div A □ and Div B □ MCR sees AGS Reachback Latch on CD pg	DISABLED ON OFF OK
Check for	acceptance of test Verify Critical Device, PSWarc20 and PSWarc8, F	Reachback

1.3	Ve	rify that unde	r power Critical Device: PSWarc20 and PSWarc8 a	are disabled with bro	oken Keytree
		VERIFY	CD Key switch is set for		XY ARC
		PLACE	Peer 5 in Mode 24		
		VERIFY	Peer 5 is in No Access		MODE 24
		VERIFY	MCR sees Inj CD		ENABLED
	П	VERIFY	MCR sees ATR inhibit Div A □ and Div B □		OFF
		TURN ON	PSWarc20 and bring up to ~100 mA		OII
		EXIDA			
		TURN	Any key in ATR keytree		
		VERIFY	MCR sees Inj CD on CD pg		DISABLED
		VERIFY	MCR sees ATR inhibit Div A \square and Div B \square		ON
		VERIFY	MCR sees Peer 5 is in		MODE 2
		RESET	All Peer 5 trips		
		PLACE	Peer 5 in Mode 24		
		VERIFY	Peer 5 is in No Access		MODE 24
		VERIFY	MCR sees Inj CD on CD pg		ENABLED
		VERIFY	MCR sees ATR inhibit Div A □ and Div B □		OFF
		TURN ON	PSWarc20 and bring up to ~100 mA		
		TURN	Any key in ATR keytree		
		VERIFY	MCR sees Inj CD on CD pg		DISABLED
		VERIFY	MCR sees ATR inhibit Div A \square and Div B \square		ON
		VERIFY	MCR sees Peer 5 is in		MODE 2
		RESET	All Peer 5 trips		
		PLACE	Peer 5 in Mode 8		
		VERIFY	Peer 5 is in Restricted Access		MODE 8
	☐ Check for acceptance of Verify that under power Critical Device: PSWarc20 and PSWarc8 are disabled with broken Keytree				SWarc8 are
			END OF TEST PROCEDURE		
TTL:	Sign	n for completion	on of initial testing:		
				Date://	·
renesse.	a.	0	0.00		
TTL:	Sign	i for completi	on of final testing:		
				Date:/	/